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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,451	07/12/2004	Nikila KRISHNAMOORTHY	TI-36271	4450

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 10/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,451	KRISHNAMOORTHY ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *17 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,13 and 14* is/are rejected.

7)☒ Claim(s) *10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 remain pending in the current application and have been examined. Claims 1, 2, 7, 8, and 12 have been amended.

2. The claim objection on page 2, item 2 of the Previous Office Action of Record has been withdrawn due to the Applicants' amendment filed 08/17/2006. However, the 35 U.S.C. 112, second paragraph rejection is only partially withdrawn due to Applicants' not correcting one of the antecedent on line 7 of claim 12. This is outlined in the new 35 U.S.C. 112, second paragraph rejection below.

Declaration Under 37 CFR § 1.131

3. The Affidavit and accompanying Exhibits A and B filed on 08/17/2006 under 37 CFR 1.131 has been considered but is ineffective to overcome the Mangum reference. The evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of the Mangum reference to either a constructive reduction to practice or an actual reduction to practice. The Affidavit has included all the facts but the exhibit fails to establish/support the claimed invention. The exhibit also fails to establish the due diligence from prior to the reference date of 08/08/2002 to a subsequent reduction to practice, MPEP 715.07. The only dates shown are 8/28/2002 (Exhibit A) and 02/03/2003 (Exhibit B), but by no means establish/support the claimed invention.

Response to Arguments

4. Applicant's arguments filed 08/17/2006 have been fully considered but they are not persuasive. Further, the newly added limitations have been rejected below.

As per the arguments for independent claims 1 and 7:

Applicant argues on page 8, "Thus, currently amended claim 1 facilitates testing of at least a first module and a second module involving transfer of data on a path connecting said first module to said second module. Park does not appear to teach such a feature. It does not appear that any data is being transferred among any of modules core (30), UDL (40) and core (50) (See Figure 1 of Park)". The Examiner agrees with the Applicants' observation of Fig. 1 of Park not explicitly showing data lines connected between any of modules core (30), UDL (40) and core (50) for the transfer of data. However, the Examiner would like to point out that Park's invention is a scan signal converting circuit to generate scan signals to test cores adopting various scan styles. The Examiner contends that the connections between the cores would inherently be there, even though not shown in Fig. 1, for the transfer of data since the test cores are part of a System on Chip (SoC) and it would be obvious to one skilled in the art that these cores would talk to each other (i.e. transfer data between the cores).

Applicant argues on page 8, "there appears to be no teaching or suggestion in Park that a "second module" is provided "with a capability of being tested in each of said plurality of characteristics of said first control signal" The Examiner disagrees and asserts that, given the broadest interpretation of this claim limitation, Park teaches that "second module" (UDL 40) is capable of being tested in each of said plurality of

characteristics of said first control signal (SCK-IN). UDL 40 uses test clock SCK which is derived from "a plurality of characteristics" of SCK-IN (said first control signal).

It is the Examiner's conclusion that independent claims 1 and 7 are not patentably distinct or non-obvious over the prior arts of record namely, Park et al. (US-6742151B2) in view of Mangum et al. (US-6744285B2). Therefore, the rejection is maintained. Based on their dependency on independent claims 1 and 7, claims 2-6 and 8, 9, 11, 13 and 14, respectively, stand rejected.

Claim Objections

5. Claims 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 and 7:

These claims recite the limitation "...even when said second module is designed for operation using a characteristic of said first control signal which is different from said

characteristic of said first control signal using which said first module is designed to operate". The phrase "which is different from said characteristic of said first control signal using which said first module is designed to operate" renders these claims indefinite because "using which said first module is designed to operate" is incomprehensible.

Claims 2-6 and 8-14:

These claims are also rejected because they depend on claims 1 and 7 and have the same problems of indefiniteness.

Clam 12:

This claim recites the limitation "said original control signal" on line 7. There is insufficient antecedent basis for this limitation in the claim. For reason for examination the Examiner will read "said original control signal" as "said first control signal". Correction is required in response to this Office Action.

Further, claim 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-9, 11, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US-6742151B2), hereinafter Park, in view of Mangum et al. (US-6744285B2), hereinafter Mangum.

Claims 1 and 7:

Park teaches a plurality of modules (core 30, user defined logic (UDL) 40, Fig. 1) in an integrated circuit (integrated circuit 1, Fig. 1), said plurality of modules comprising a first module (core 30, Fig. 1) and a second module (user defined logic (UDL) 40, Fig. 1), wherein data is transferred on a path connecting said first module to said second module (inherently there as per arguments above), wherein said first module and said second module are to be operated together during said testing such that said second module operates using a second one of a plurality of characteristics (SCK) of a first control signal (Scan Clock, SCK-IN, Fig. 1) when said first module is operated using a first one of said plurality of characteristics (MCK) of said first control (Scan Clock, SCK-IN, Fig. 1). Park also teaches a second module (user defined logic (UDL) 40, Fig. 1) provided with a capability of being tested in each of a plurality of characteristics of said first control signal (Scan Clock, SCK-IN, Fig. 1). Park further teaches said testing is facilitated even when said second module (user defined logic (UDL) 40, Fig. 1) is designed for operation using a characteristic of said first control signal (SCK) which is different from said characteristic of said first control signal using which said first module is designed to operate (MCK). (Col. 5, l. 28 to col. 7, l. 10).

Park does not explicitly teach "a test logic being programmable to generate a derived control signal having a desired characteristic, wherein said derived control

signal is generated from said first control signal, and wherein said derived control signal of said desired characteristic is provided as a control signal to said second module and said second module is tested with said desired characteristic of said first control signal by programming said test logic". However, Park does teach a test logic (a scan signal converting circuit 100, Fig. 1 and 2) to generate a derived control signal (SCK, Fig. 1 and 2), wherein said derived control signal (SCK, Fig. 1 and 2) is generated from said first control signal (Scan Clock, SCK-IN, Fig. 1). Park also teaches the first scan signal converting circuit 110 includes first delay cell 111. The delayed clock signals from the first delay 111 is then input to the UDL 40 as the output scan clock signal SCK. (Fig. 2, col. 6, ll. 22-23, 45-61).

Mangum teaches in an analogous art "test logic (phase-alignment system) being programmable to generate a derived control signal" in that the phase-alignment system comprises a user interface 60 that provides a user with a mechanism by which the phase-alignment circuits 40 and 50 can be controlled. Each of the phase-alignment circuits 40 and 50 comprises delay elements that have known delay times. The phases of clocks A and B can be varied by adjusting the number of delay elements in the paths of clocks A and B or by adjusting the number of delay elements in the path of the reference clock. The placement of the delay elements in the clock paths is controlled by the user through the user interface. Mangum also teaches, in reference to Fig. 4, the number of delay elements that are placed in the clock paths is controlled (**test logic being programmable**) by the select lines 74, "SELECT_A_DELAY", and 75, "SELECT_REF_DELAY", which are controlled (i.e. programmed) by the user via the

user interface 60. The select lines 74 and 75 are each multi-bit lines that are received by multiplexers A 76 and B 77. The number of delay elements that are connected in series with the clock lines depends on the bit values that are delivered to the multiplexers 76 and 77. (Col. 3, l. 49 to col. 4, l. 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Park's first delay cell 111 with Mangum's phase-alignment circuit 40. The artisan would be motivated to do so because it would enable Park control the phases or edges of the control signals based on a programmed bit pattern from Mangum's user interface.

Claims 2 and 8:

Park teaches "said desired characteristic is determined to test said path at a same speed as in a functional mode" in that in Fig. 4 Park illustrates the generated test clocks SCK and CK is the same frequency as the external clocks SCK-IN and CK-IN, thus testing the first module and the second module at the same speed as in functional mode.

Claims 3 and 9:

Park in view of Mangum teaches "said first control signal (Scan Clock, SCK-IN, Fig. 1) comprises a clock signal". Park in view of Mangum does not explicitly teach said test logic can be programmed to generate said derived control signal as an inverted signal of said clock signal". However, Park in view of Mangum does teach phase-alignment circuit 40 can be programmed to vary the amount of delay on a particular clock signal in effect changing the phase. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the derived control signal (SCK,

Fig. 1 and 2) can be delayed such that it becomes 180 degrees out of phase with the first control signal (Scan Clock, SCK-IN, Fig. 1). The artisan would be motivated to do so because this programming would effectively invert the derived control signal (SCK, Fig. 1 and 2).

Claims 4 and 11:

Park in view of Mangum does not explicitly teach "said first control signal comprises a scan enable signal and wherein said programmable field can be set to generate said derived control signal as rising edge triggered or falling edge triggered scan enable signal". However, Park in view of Mangum does teach, as per the rejection of claims 3 and 9 above, the derived control signal (SCK, Fig. 1 and 2) can be delayed such that it becomes 180 degrees out of phase with the first control signal (Scan Clock, SCK-IN, Fig. 1), effectively inverting the derived control signal (SCK, Fig. 1 and 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Mangum's phase-alignment circuit 40 can be programmed to vary the amount of delay on any particular signal (i.e. clock, scan enable) in effect changing the phase. The artisan would be motivated to do so because this would enable Park in view of Mangum to introduce enough delay in the derived control signal (i.e. scan enable) such that it becomes a rising edge triggered or falling edge triggered signal.

Claims 5 and 13:

Park in view of Mangum teaches "said test logic (a scan signal converting circuit 100, Fig. 1 and 2) comprises a register (Mangum's MUX A and B, Fig. 4) which can be programmed".

Claims 6 and 14:

Park teaches said first module comprises a core module (core 30, Fig. 1) provided by a third party not designing said integrated circuit, and said second module is designed by a designer designing said integrated circuit (user defined logic (UDL) 40, Fig. 1).

Allowable Subject Matter

8. Claims 10 ands 12 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to testing of integrated circuits, and more specifically to a method and apparatus for testing of modules operating with different characteristics of control signals using scan based techniques.

The claimed invention as set forth in claim 10 recites features such as: test logic that comprises a bit indicating whether said derived control signal is to be generated as a positive clock signal or a negative clock signal and an XOR logic gate receiving said bit and said clock signal and generating said derived control signal.

The prior arts of record teach a scan signal converting circuit 100 (i.e Park in view of Mangum) that can be programmed via user interface 60 to vary the delays as to change the phase of clock signals used for different modules (core 30, UDL, Fig. 1 of Park); Park et al. (US-6742151B2) and Mangum et al. (US-6744285B2) are examples of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, the limitations of claim 10, namely *the bit* indicating whether said derived control signal is to be generated as a positive clock signal or a negative clock signal and the *XOR logic gate* that receives *the indicating bit* and the clock signal to generate the derived control signal. As such, modification of the prior art of record to include the claimed *indicating bit* and *XOR logic gate* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *indicating bit* and *XOR logic gate* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *indicating bit* and *XOR logic gate* as set forth in claim 10.

Note: The ***bolded/italics/underlined*** words in claim 12 below are the anticipated corrections as per the 35 U.S.C. 112, 2nd paragraph, rejection above.

The claimed invention as set forth in claim 12 recites features such as: test logic that comprises a bit indicating whether said derived control signal is to be generated as said rising edge triggered or said falling edge triggered scan enable signal, a flip-flop coupled to receive said ***first*** control signal and being clocked on an inverted clock signal and a multiplexor selecting either the output of said flip-flop or said first control signal under the control of said bit.

The prior arts of record teach a scan signal converting circuit 100 (i.e Park in view of Mangum) that can be programmed via user interface 60 to vary the delays as to

change the phase of clock signals used for different modules (core 30, UDL, Fig. 1 of Park); Park et al. (US-6742151B2) and Mangum et al. (US-6744285B2) are examples of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, the limitations of claim 12, namely *the indication bit*, *the flip-flop* and *multiplexor.* As such, modification of the prior art of record to include the claimed *indication bit*, *the flip-flop* and *multiplexor* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *indication bit*, *the flip-flop* and *multiplexor* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *indication bit*, *the flip-flop* and *multiplexor* as set forth in claim 12.

Hence, claims 10 and 12 are allowable over the prior arts of record.

The Examiner agrees with the Applicant's arguments with regard to this feature in view of the arts of record; therefore, the Examiner favors the allowance of claims 10 and 12. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 10/25/06

John J. Tabone, Jr.
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